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C I P E

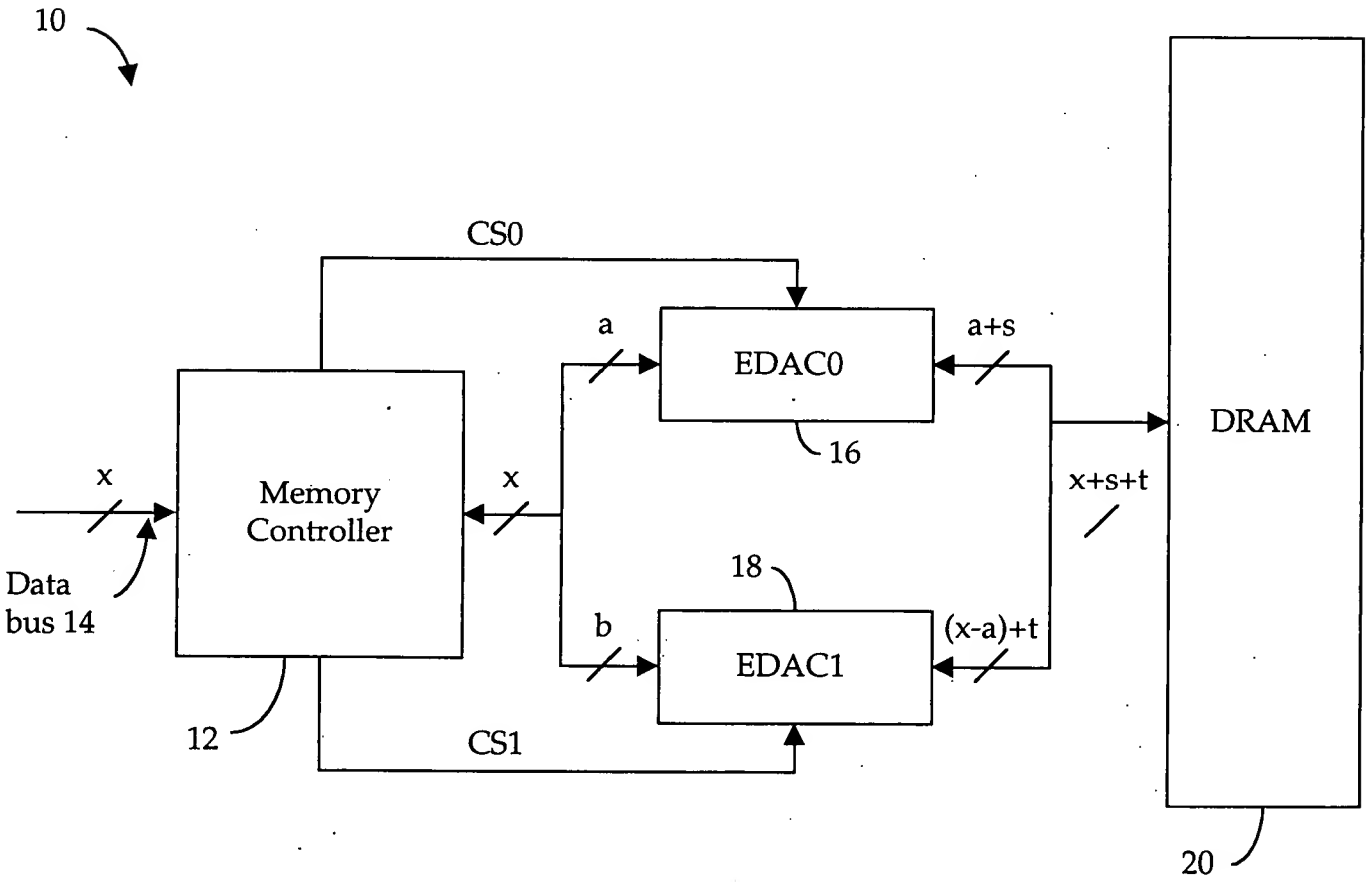

FIG. 1

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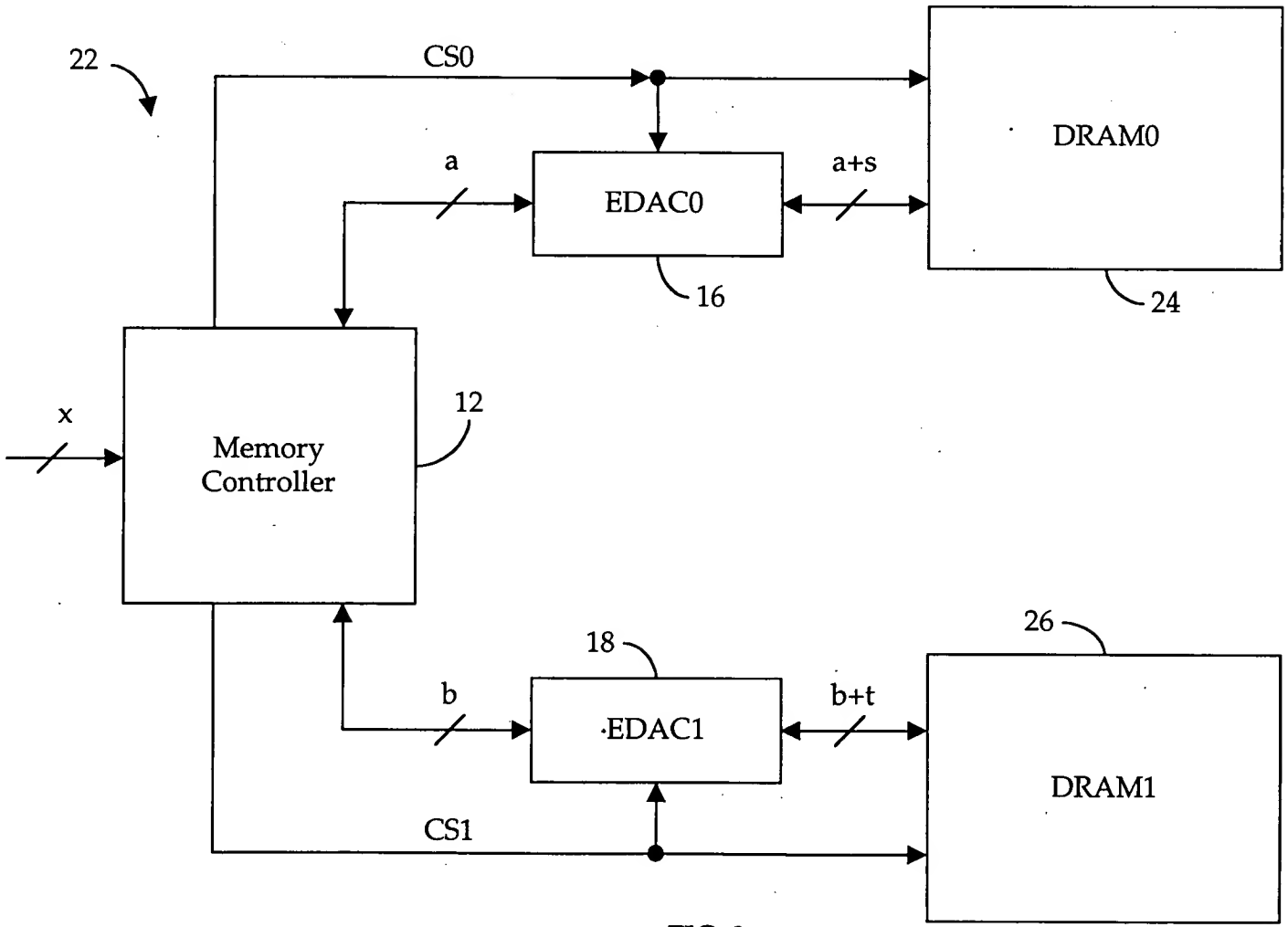

FIG. 2

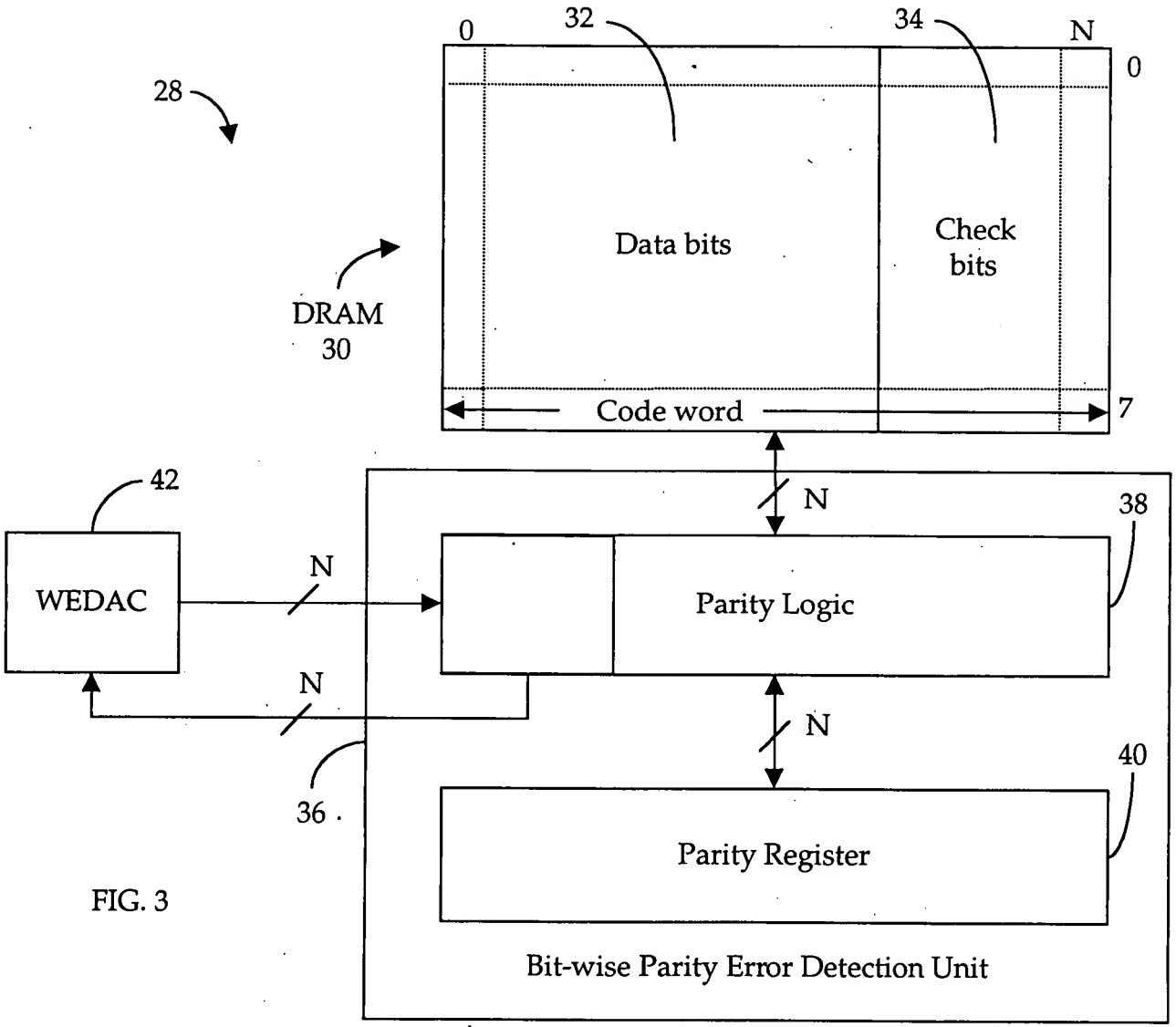
28
DRAM
30
0
32
34
N
0
Data bits
Check
bits
Code word
7
N
38
42
WEDAC
N
Parity Logic
N
N
40
36
Parity Register
Bit-wise Parity Error Detection Unit

FIG. 3

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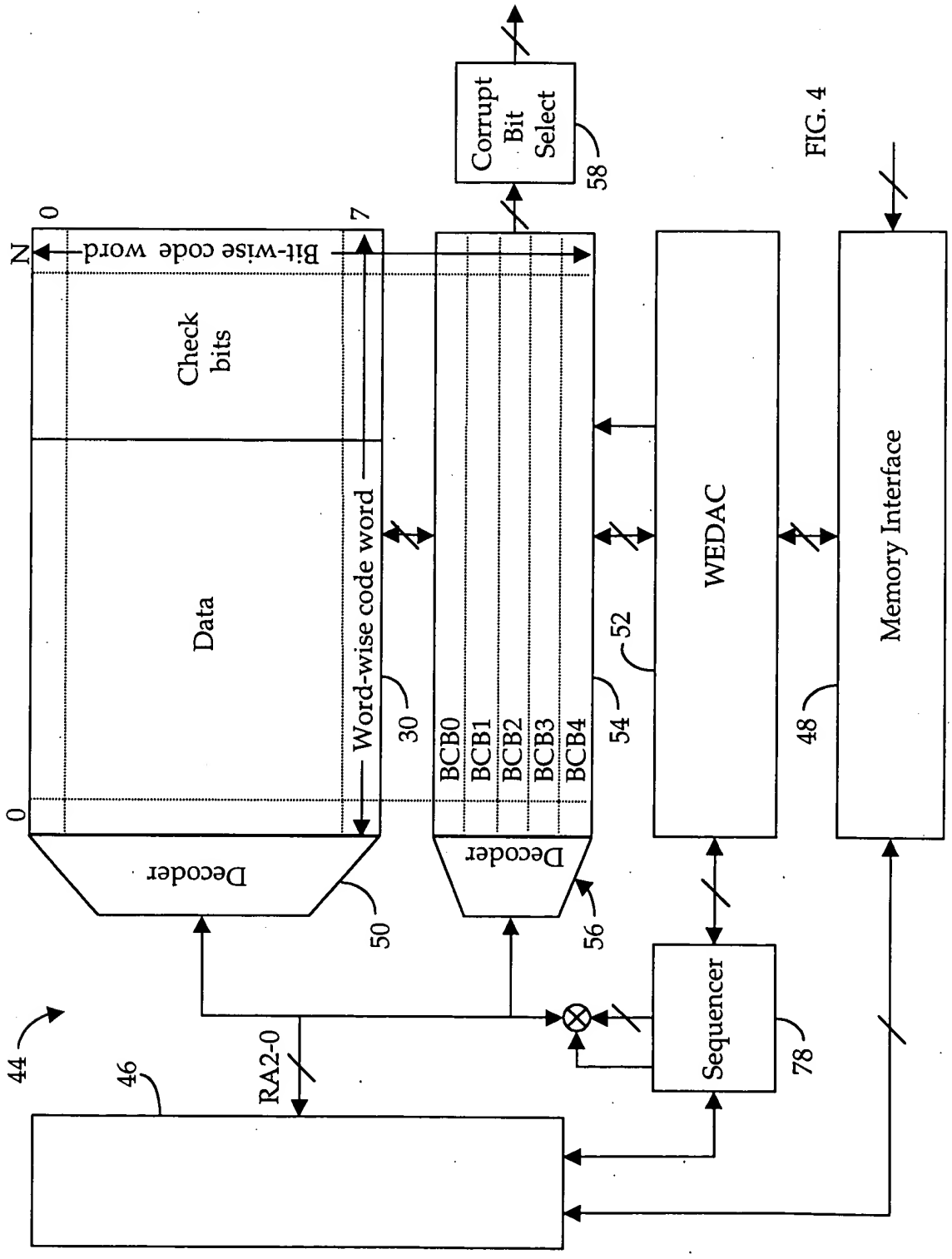

FIG. 4

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	ROW0	ROW1	ROW2	ROW3	ROW4	ROW5	ROW6	ROW7	
CLEAR	X	X	X	X		X			CCBS0
CLEAR	X	X	X				X	X	CCBS1
CLEAR	X			X	X		X	X	CCBS2
CLEAR		X		X	X	X	X		CCBS3
SET			X		X	X		X	CCBS4

FIG. 5A

	RA2	RA1	RA0	CCBS4	CCBS3	CCBS2	CCBS1	CCBS0
ROW0	0	0	0	0	0	1	1	1
ROW1	0	0	1	0	1	0	1	1
ROW2	0	1	0	1	0	0	1	1
ROW3	0	1	1	0	1	1	0	1
ROW4	1	0	0	1	1	1	0	0
ROW5	1	0	1	1	1	0	0	1
ROW6	1	1	0	0	1	1	1	0
ROW7	1	1	1	1	0	1	1	0

FIG. 5B

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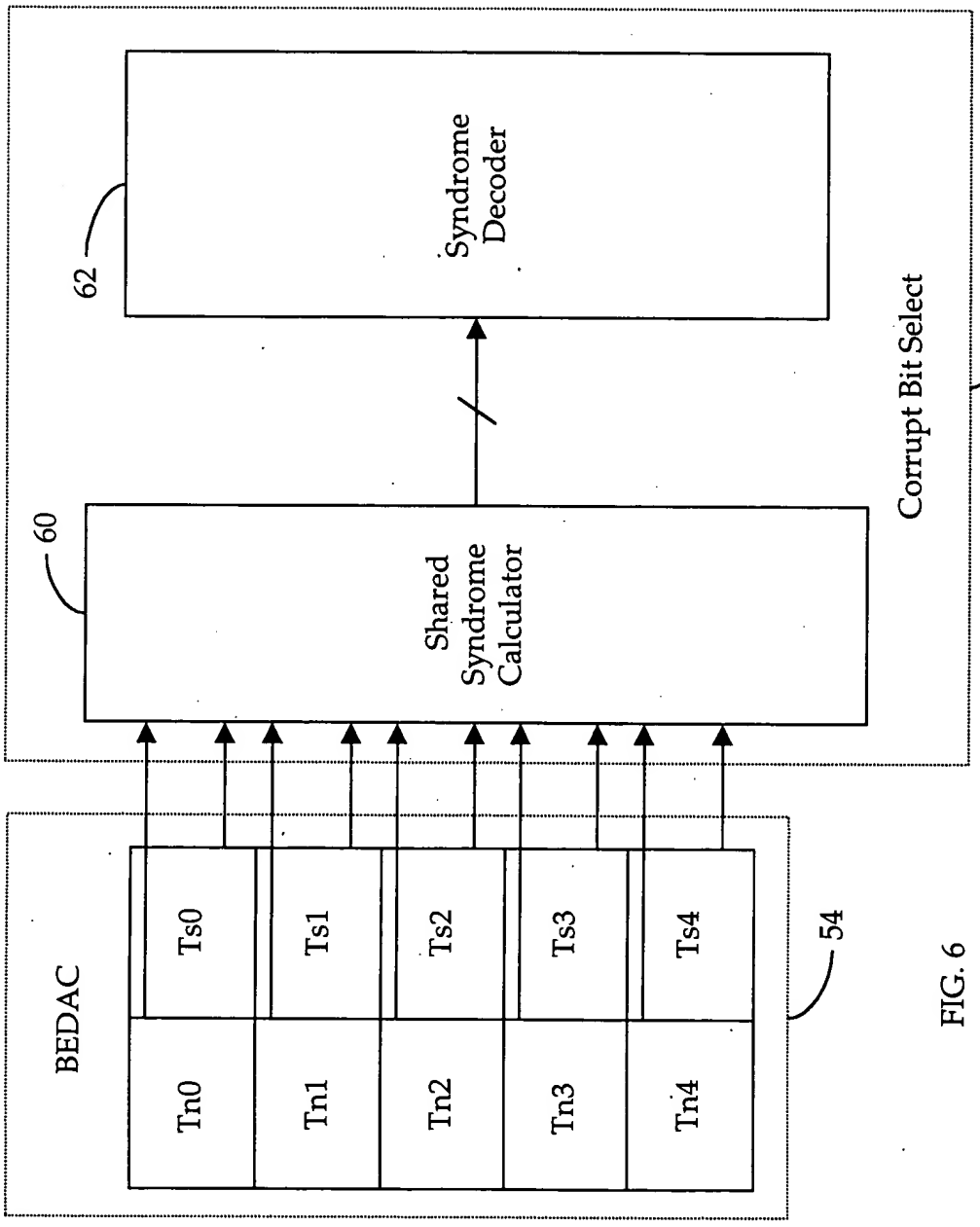

FIG. 6

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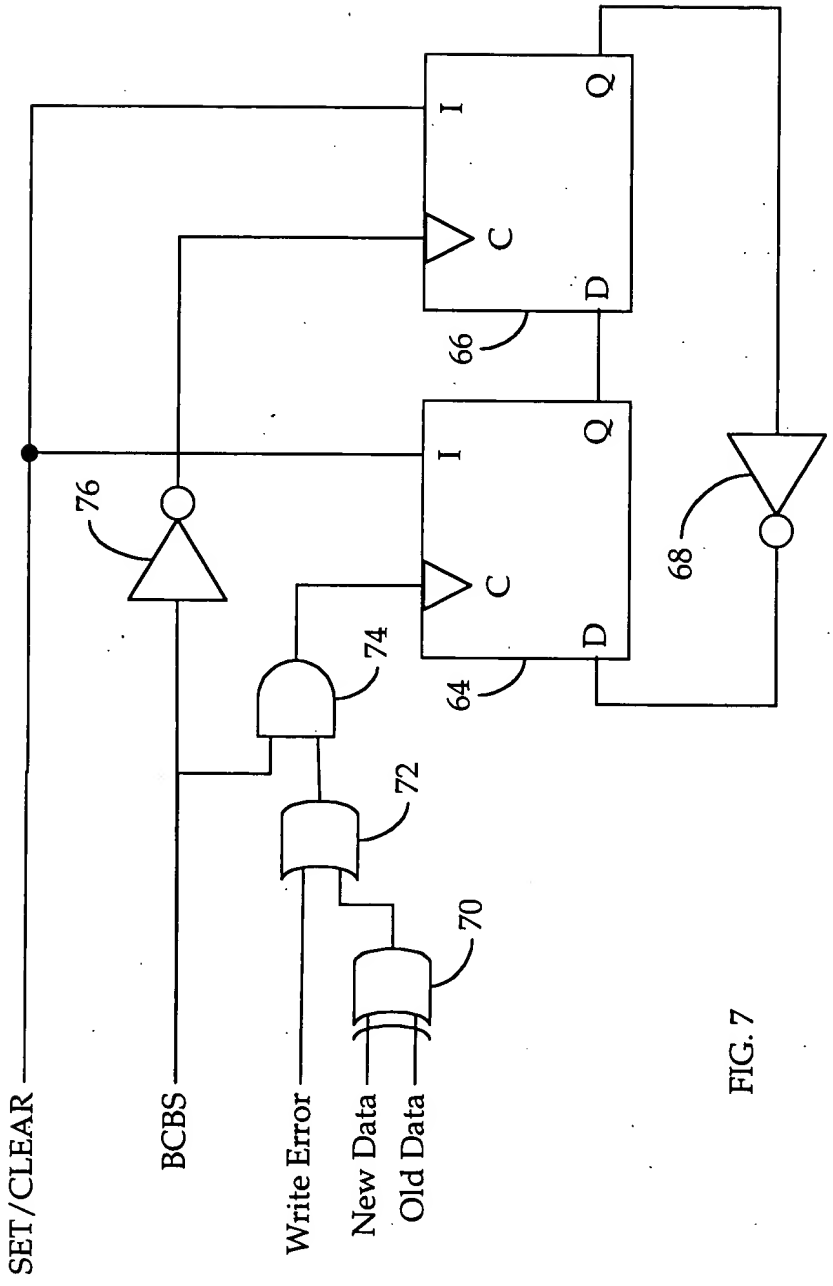

FIG. 7

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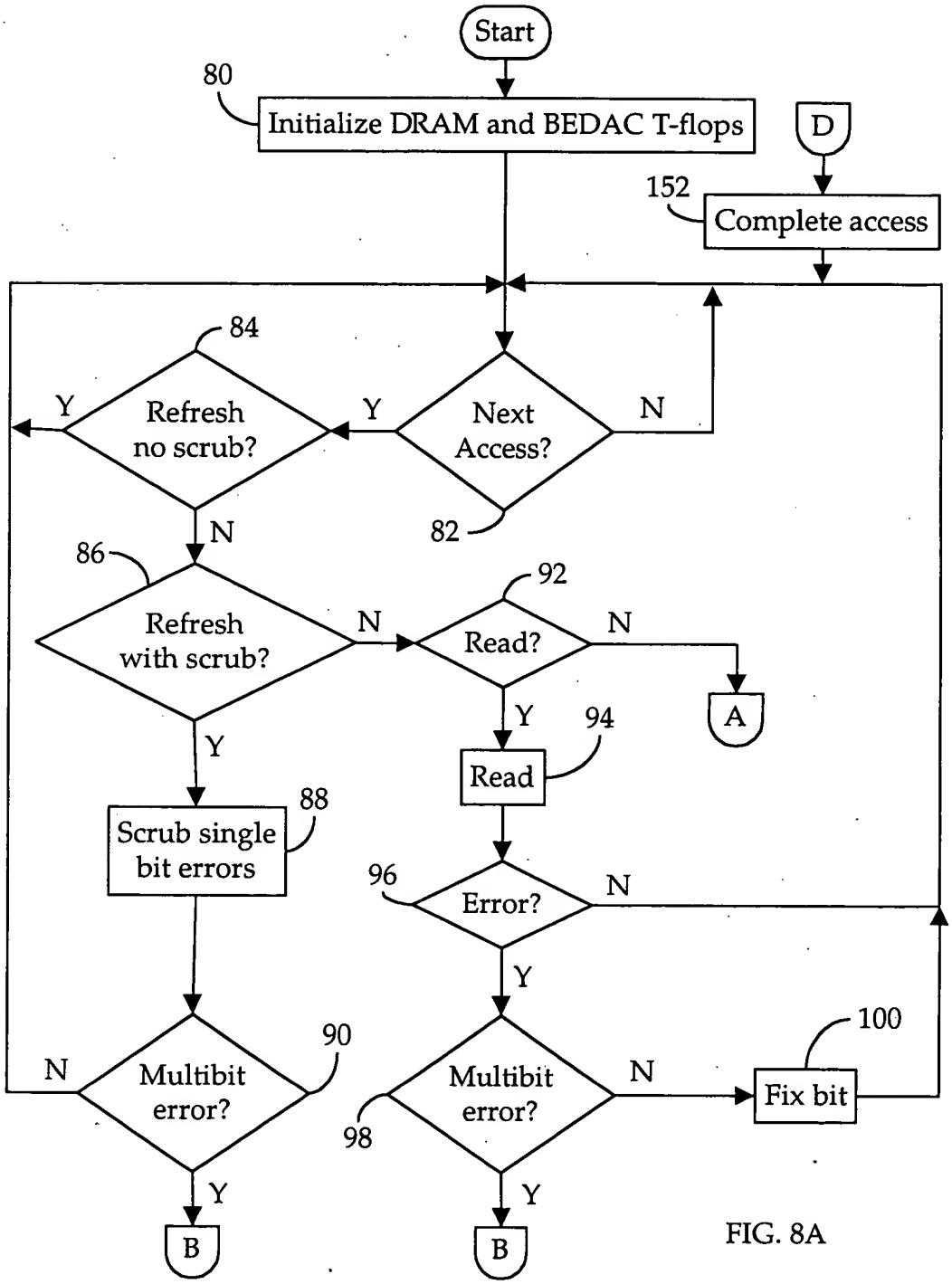

FIG. 8A

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JC09

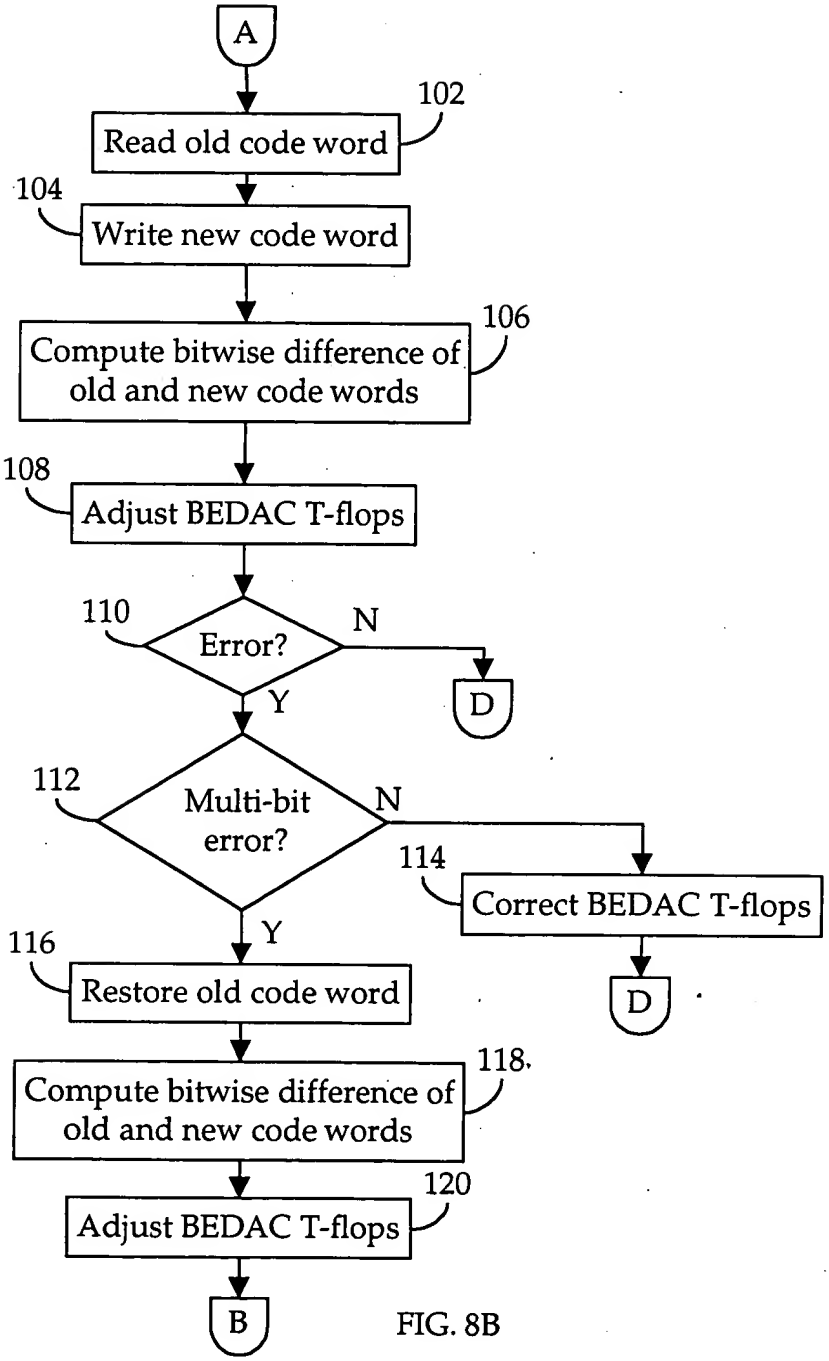

FIG. 8B

OIPE
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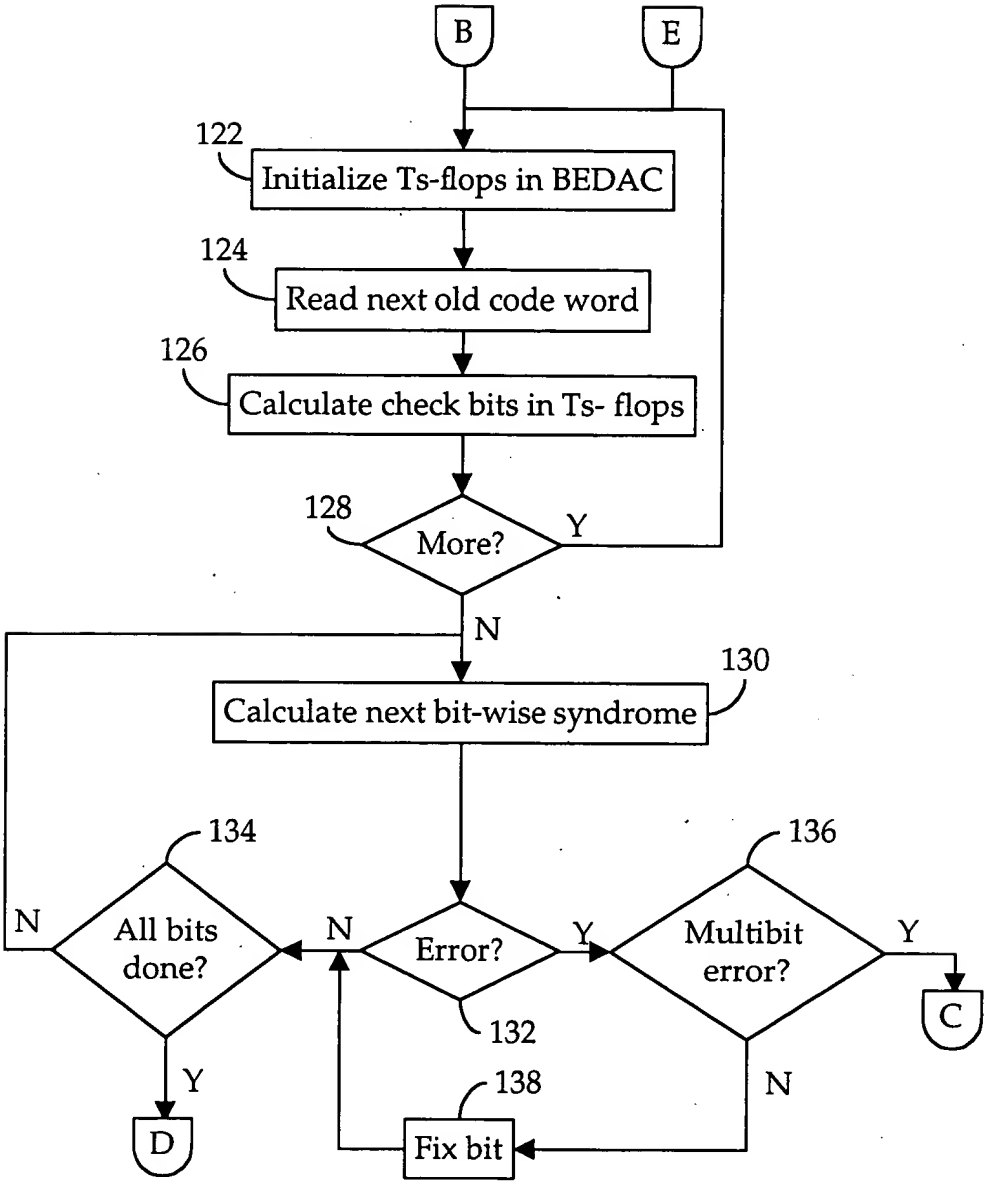

FIG. 8C

OIPE
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PATENT & TRADEMARK OFFICE
JC09

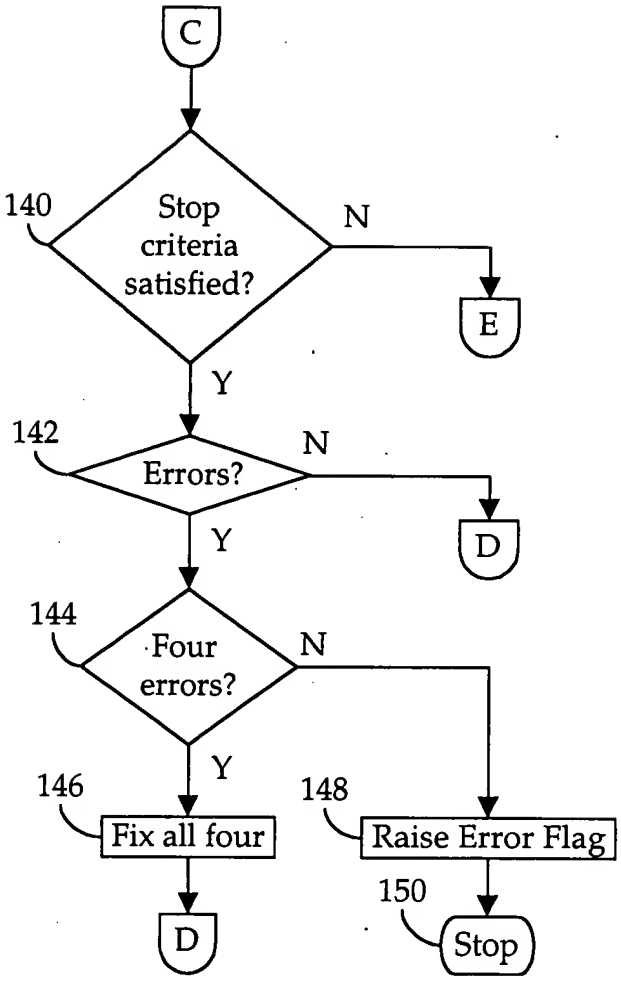

FIG. 8D

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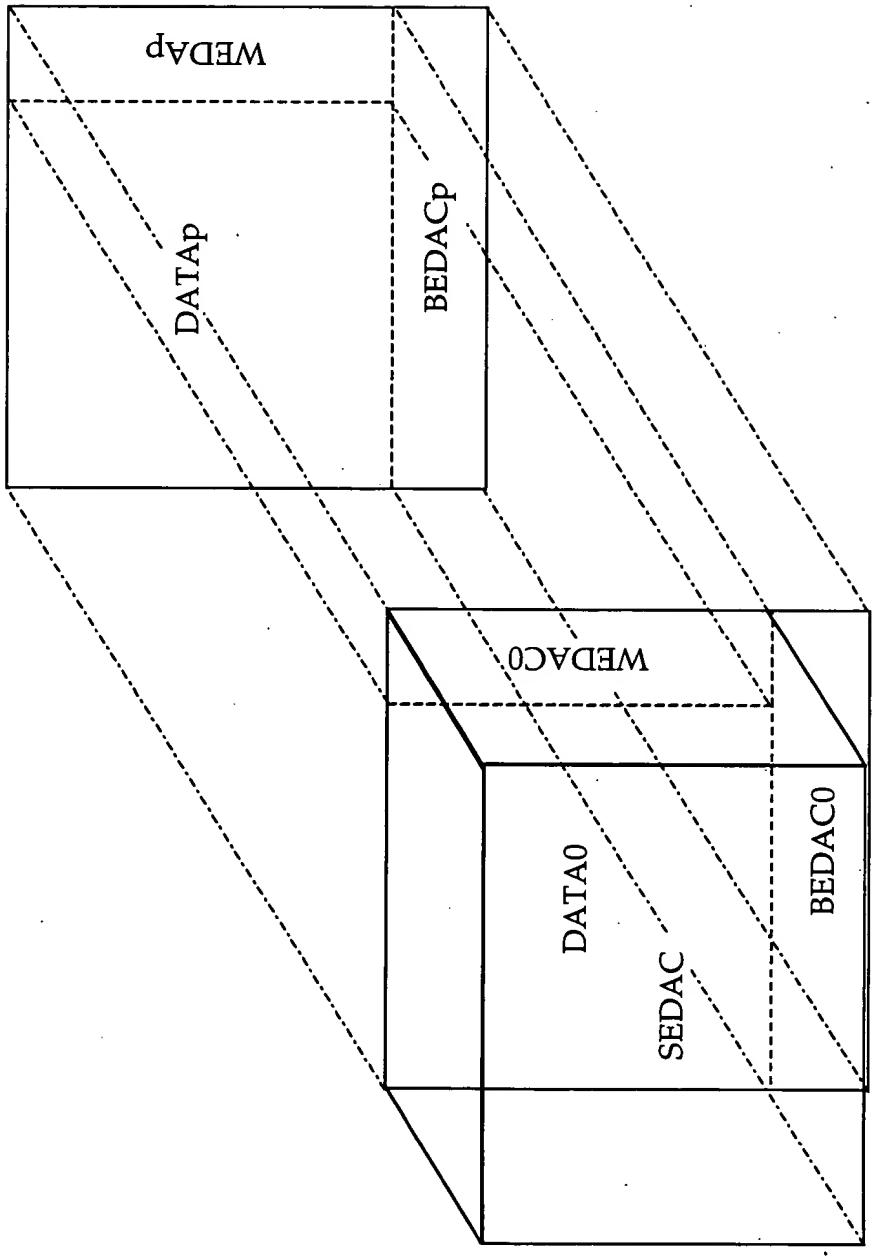

FIG. 9